Remarks

In the Office Action mailed February 24, 2004:

1. Claims 1-3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,574,758 (Eccles);
2. Claims 4-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eccles, in view of U.S. Patent No. 5,349,587 (Nadeau-Dostie);
3. Claims 9-10, 17 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eccles, in view of U.S. Patent No. 5,023,590 (Johnson); and
4. Claims 11-16, 18-19 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eccles, in view of Johnson and Nadeau-Dostie.

I. U.S. Patent No. 6,574,758 (Eccles)

Eccles is directed to "Testing a Bus Coupled Between Two Electronic Devices" (title), and therefore cannot make obvious all elements of Applicant's invention.

A. Eccles Requires Multiple Circuits and a Bus

As specified in the Title, the Summary (column 1, lines 29-33) and elsewhere (e.g., column 2, lines 60-65), Eccles deals with testing a *bus*, and requires *multiple* independent circuits – one to generate and send a test signal across the bus, and another to generate a verifying signal and compare it to the test signal.

In contrast, Applicants' invention is directed at a *single* circuit that is *self-testable*. No external circuits are required, and the circuit tests its own I/O interface, not an external bus. Eccles thus teaches away from the present invention.

In both the FIG. 2 and FIG. 4 implementations of Eccles, neither circuit is self-testable. In particular, because Eccles is specifically designed to test a bus, neither circuit *can* be self-testable. The test signals must be conveyed by one circuit and received by another. Thus, in neither implementation can a single circuit *generate* a test signal, *transmit* and *receive* that signal across its I/O interface, and then *compare* the received signal to the test signal.

The Examiner cited column 6, lines 39-43 and FIG. 4 of Eccles as suggesting an ASIC chip having a built-in self-test DDR circuit. However, the FIG. 4 implementation does not test an I/O interface of the circuit. If the FIG. 4 implementation is on one ASIC chip, then it is

merely testing an internal trace, not an external interface as recited in claims of the present application.

Applicant therefore asserts that a person skilled in the art and seeking a method or apparatus for a self-testing Double Data Rate (DDR) circuit would not look to Eccles.

II. Nadeau-Dostie (U.S. Patent No. 5,349,587)

Nadeau-Dostie is directed to methods and apparatus for testing a digital system (Abstract), particularly those using multiple clock rates (Title).

A. Nadeau-Dostie Cannot Self-Test an I/O Interface

As with Eccles, Nadeau-Dostie does not provide a circuit capable of self-testing an input/output interface of the circuit. The digital system 100 that is tested in Nadeau-Dostie (FIG. 3) is a single integrated circuit (column 5, lines 58-59). In particular, the portion that is tested is a combinational network 20 connected to sets of scannable memory elements 10 (FIG. 2; column 3, lines 60-63). As shown in FIG. 3, the tested network is completely contained within the single integrated circuit; thus, there can be no self-testing of an external I/O interface.

In contrast, in claimed embodiments of the invention (e.g., claim 1), a DDR circuit self-tests its own I/O interface. One skilled in the art would not look to Nadeau-Dostie for assistance in this area.

III. Selected Claims

A. Claims 1-8, 23

Claim 1 was amended to make it clearer that the DDR circuit self-tests its I/O interface, as opposed to a bus tested in the FIG. 4 implementation of Eccles. As described above in Section I.A, Eccles' FIG. 4 implementation does not test an external I/O interface; and neither Eccles' FIG. 2 nor FIG. 4 implementations self-test a single circuit – they both require two circuits.

Claim 23 was added to make it clearer that, in the embodiment of the invention recited in claim 1, a test signal need not be received by an external circuit. As explained above, Eccles requires *multiple* circuits in order to test a bus connecting the circuits.

B. Claims 9-16

Claim 9 has been amended to make it clearer that the input/output interface recited in the claim is an *external* interface. As described in Section I.A, Eccles does not teach or suggest this. One implementation of Eccles (i.e., FIG. 2) requires two separate circuits, on separate chips, for testing a bus connecting the circuits. Another implementation (FIG. 4), even if able to be configured on a single chip, can only test a wholly internal bus.

C. Claims 17-22

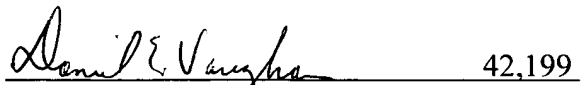
Claim 17 has been amended to make it clearer that the input/output interface recited in the claim is an *external* interface. As described in Section I.A, Eccles does not teach or suggest this. One implementation of Eccles (i.e., FIG. 2) requires two separate circuits, on separate chips, for testing a bus connecting the circuits. Another implementation (FIG. 4), if able to be configured on a single chip, can only test a wholly internal bus.

CONCLUSION

No new matter has been added with the preceding amendments. It is submitted that the application is in suitable condition for allowance. Such action is respectfully requested. If prosecution of this application may be facilitated through a telephone interview, the Examiner is invited to contact Applicant's attorney identified below.

Respectfully submitted,

Date: May 6, 2004

By:  42,199
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